UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,919	02/28/2002	Albrecht Mayer	J&R-0819	1176

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EXAMINER
BRITT, CYNTHIA H

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.
2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.
   4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-11* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.
   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a)☒ All   b)☐ Some * c)☐ None of:
   1.☒ Certified copies of the priority documents have been received.
   2.☐ Certified copies of the priority documents have been received in Application No. _____.
   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).
   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date *5*.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

⁻ DETAILED ACTION

Claims 1-11 are presented for examination.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which

papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on February 28, 2002 has

been considered by the examiner. Form 1449 has been signed and returned with this

office action.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show

every feature of the invention specified in the claims. Therefore, the method of claims

8-11 must be shown or the feature(s) canceled from the claim(s). No new matter should

be entered.

The examiner would like to point out that method claims are typically illustrated

by a simple flowchart(s) with the boxes containing the steps of the method. These

drawings aid in the understanding of the claimed invention.

A proposed drawing correction or corrected drawings are required in reply to the

Office action to avoid abandonment of the application. The objection to the drawings

will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, and 3-7, are rejected under 35 U.S.C. 102(e) as being anticipated

by Churchill et al. U.S. Patent No. 6,006,347.

As per claims 1 and 4, Churchill et al. teach a *programmable scan interface*

which provides a mechanism for *programmably altering various signals* within the

SRAM to improve the observability and characterization of circuitry within the SRAM.

The programmable scan interface may output from one to n control signal(s). Control

line(s) may comprise from one to n lines (or from one to n/m lines, where m is the value

of an m-to-1 multiplexer coupling the control signals from the programmable scan

interface to control line(s)) or busses. One of the control signals may configure the

output register to become transparent; that is, the output register may switch from

synchronous to asynchronous operation, such that data may be passed directly through

the output register. This may increase the ability to monitor and *test the operation of the*

memory core without interference and/or masking effects caused by the output register.

One or more of the control signals may also be coupled to the input register to configure

the input register to become transparent. The programmable scan interface may be

programmed to alter the various signals or functions of the SRAM *in response to a*

number of input signals that may be supplied from external pins on the SRAM. These

pins may be dedicated pins, no-connect (NC) pins with hidden functions, pins that

multiplex the *scan path test mode functions* with other functions for the SRAM, etc.

These signals may include a serial input data signal S1, a serial timing signal (e.g.,

SCLK), a scan mode activation enable signal (e.g., SE), and a test mode activation

enable signal (e.g., TM). Errors can be observed at the output of the output register.

(Column 4 lines 47-65, Column 5 lines 24-35, Column 7 lines 50-51, Column 13, lines 1-

7, figure 2)

As per claims 3 and 5, Churchill et al. teach *disabling the clock* on specified scan

lines such that data is not shifted into the scan register. Additionally, scan data is not

output to the decode logic as the enable input is inactive. One or more scan bits may

activate a bypass, transparency, or flow-through circuit in the *clock generator circuit* to

output the external periodic signal (CLK) rather than generating an internal clock signal

(Column 6 lines 9-15, Column 7 lines 1-12, Figure 3)

As per claims 6 and 7, Churchill et al. teach that the scan path circuitry includes a

programmable scan test interface that has test mode pins and a protocol for using these

test mode pins to control whether an integrated circuit loads or outputs scan test data,

enters a test mode defined by the scan test data, or operates in a normal fashion (e.g.,

is configured to conventionally read data from and/or write data to the memory core).

Column 3 lines 21-29

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8, 10, and 11 are rejected under 35 U.S.C. 102(b) as being

anticipated by Smith U. S. Patent No. 5,642,363.

As per claim 8, Smith teaches a method of testing for errors using scan chains

Scan Control ASIC can dynamically configure the electronic paths, or scan paths, that

are to be tested. By properly connecting the outputs of the Master TAP ASIC to a

switchable input of the Scan Control ASIC, the scan path can be dynamically

reconfigured during the test to shorten test time. Once the input of the test interface is

connected to the diagnostic processor, and a master output of the test interface is

connected to a switchable input of a circuit, step 62 represents the *diagnostic processor*

commanding the circuit to configure the scan paths on the electronic assembly into one

virtual scan path. Once this is done, step 64 represents the diagnostic processor

sending data to the electronic assembly. Finally, after the configuration that was

configured in step 62 is *completely tested,* and *some portion of the virtual scan path can*

be removed from the scan path for the remainder of the test, step 66 represents the

diagnostic processor reconfiguring the assembly for the test to continue. This process

repeats itself until all of the scan paths have been tested on the assembly. (Column 2

lines 32-41, Column 4 lines 53-67, Figure 3)

As per claims 10 and 11, Smith teaches a diagnostic controller, which generates

the commands to be sent to the assembly, receives data from the assembly, and

compares that data with expected values. Once a path is tested and passes the test,

the test path is reconfigured by the diagnostic processor to break the path at nodes,

which will reconfigure and remove subassemblies from the test path as much as

possible. This ensures that the testing will test paths in an orderly fashion, as well as

testing the paths a minimal number of times. (Column 2 lines 42-49, Column 4 lines 30-

40)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.

  2. Ascertaining the differences between the prior art and the claims at issue.

  3. Resolving the level of ordinary skill in the pertinent art.

  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill et al. U.S. Patent No. 6,006,347 in view of Barbier et al. U. S. Patent No. 5,777,489.

As per claim 2, Churchill et al. substantially teach the claimed invention in which a *programmable scan interface* which provides a mechanism for *programmably altering various signals* within the SRAM to improve the observability and characterization of circuitry within the SRAM. The programmable scan interface may output from one to n control signal(s). Control line(s) may comprise from one to n lines (or from one to n/m lines, where m is the value of an m-to-1 multiplexer coupling the control signals from the programmable scan interface to control line(s)) or busses. One of the control signals may configure the output register to become transparent; that is, the output register may switch from synchronous to asynchronous operation, such that data may be passed directly through the output register. This may increase the ability to monitor and *test the*

operation of the memory core without interference and/or masking effects caused by the output register. One or more of the control signals may also be coupled to the input register to configure the input register to become transparent. The programmable scan interface may be programmed to alter the various signals or functions of the SRAM *in response to a number of input signals* that may be supplied from external pins on the SRAM. These pins may be dedicated pins, no-connect (NC) pins with hidden functions, pins that multiplex the *scan path test mode functions* with other functions for the SRAM, etc. These signals may include a serial input data signal S1, a serial timing signal (e.g., SCLK), a scan mode activation enable signal (e.g., SE), and a test mode activation enable signal (e.g., TM). Errors can be observed at the output of the output register. (Column 4 lines 47-65, Column 5 lines 24-35, Column 7 lines 50-51, Column 13, lines 1-7, figure 2) Not explicitly disclosed is the on-chip debug support unit.

However, in an analogous art, Barbier et al. teach an FPGA having integrated debugging facilities in which an input to a trigger outside FPGA is generated whenever the stored pattern is detected. In other words, for the illustrated embodiment (figure 9), 4 logic element internal state events can be monitored simultaneously. (Column 6, lines 26-29) Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have combined the programmable scan interface of Churchill et al. with the debug circuitry of Barbier et al. This would have been obvious as suggested by Churchill et al. in order to test or monitor the state of circuitry which may be inaccessible from external pins (column 1 lines 27-35).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith

U. S. Patent No. 5,642,363 in view of IBM Technical Disclosure Bulletin (TDB-ACC-

NO) NA9003105 *"Programmable Microcoded Self-Test Apparatus for Processor*

***Cache Memory"* March 1990, US, Vol 32, Issue 10A, PAGES105-107, publication**

date March 1, 1990.

As per claim 9, Smith substantially teaches the claimed method of testing for

errors using scan chains Scan Control ASIC can dynamically configure the electronic

paths, or scan paths, that are to be tested. By properly connecting the outputs of the

Master TAP ASIC to a switchable input of the Scan Control ASIC, the scan path can be

dynamically reconfigured during the test to shorten test time. Once the input of the test

interface is connected to the diagnostic processor, and a master output of the test

interface is connected to a switchable input of a circuit, step 62 represents the

diagnostic processor commanding the circuit to configure the scan paths on the

electronic assembly into one virtual scan path. Once this is done, step 64 represents

the diagnostic processor sending data to the electronic assembly. Finally, after the

configuration that was configured in step 62 is completely tested, and some portion of

the virtual scan path can be removed from the scan path for the remainder of the test,

step 66 represents the diagnostic processor reconfiguring the assembly for the test to

continue. This process repeats itself until all of the scan paths have been tested on the

assembly (Column 2 lines 32-41, Column 4 lines 53-67, Figure 3). Not explicitly

disclosed is identifying and analyzing the detected error.

However, in an analogous art, IBM teaches that in this system, the driver

program interprets the results and *identifies failing array chips and cells if a cache array*

error was detected. The PC driver program is the interface to the microcoded array test.

It targets the processor under test and loads the diagnostic microcode and microcode

control file into local working store, initializes the Instruction, Execution, and Buffer

Control Elements, handles solicited and unsolicited responses from these elements,

and *analyzes and identifies defective modules and array chips*. It then communicates

the results of the test back to the user (Paragraphs 3 and 8). Therefore it would have

been obvious to a person having ordinary skill in the art at the time this invention was

made to have used the method of testing taught by smith with the method of identifying

and analyzing errors taught by IBM. This would have been obvious as suggested by

Smith (column 1 lines 37-50) in order to assure proper functioning of the device prior to

actual use with a minimum of time and cost expended.

Conclusion

The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

U. S. Patent No. 6,094,729   Mann

This patent teaches using an enhanced J-TAG interface access operation in

which In-circuit emulation (ICE) and software debug facilities are included in a

processor via a debug interface that interfaces a target processor to a host system. The

debug interface includes a trace controller that monitors signals produced by the target

processor to detect specified conditions and produce a trace record of the specified

conditions including a notification of the conditions are selected information relating to

the conditions. The trace controller formats a trace information record and stores the

trace information record in a trace buffer in a plurality of trace data storage elements.

The trace data storage elements have a format that includes a trace code (TCODE)

field indicative of a type of trace information and a trace data (TDATA) field indicative of

a type of trace information data.

Narayanan et al. "*Reconfiguration techniques for a single scan chain*" IEEE

Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.: 14

Issue: 6, Jun. 1995, Page(s): 750-765. Inspec Accession Number: 4975302

This patent teaches that a major drawback in using scan techniques is the long

test application times incurred in shifting test data in and out of a device. This problem

assumes even greater significance with the rapid growth in both the number of test

patterns and scan registers occurring in complex VLSI designs. This paper presents a

novel methodology based on reconfiguring a single scan chain to minimize the shifting

time in applying test patterns to a device. The main idea is to employ multiplexers to

bypass registers that are not frequently accessed in the test process and hence reduce

the overall test application time, For partitioned scan designs, two different modes of

test application which can be used to efficiently tradeoff the logic and routing overheads

of the reconfiguration strategy with the test application time are described. In each case

a detailed analysis and optimization techniques to minimize the number of added

multiplexers and the corresponding test time is provided.

S. Narayanan et al., "*Reconfigurable scan chains: A novel approach to reduce test

application time*", Proceedings of ICCAD, pp. 710-715, Sep.1993. Inspec Accession

Number: 4979762

This patent teaches that a major drawback in using scan techniques is the long

test application times needed to shift test data in and out of a device. This paper

presents a novel methodology based on reconfiguring a single scan chain to minimize

the shifting time in applying test patterns to a device. The main idea is to employ

multiplexers to bypass registers that are not frequently accessed in the test process and

hence reduce the overall test time. For partitioned scan designs, two different modes of

test application which can be used to efficiently tradeoff the logic and routing overheads

of the reconfiguration strategy with the test application time are described. In each case,

optimization techniques to minimize the number of added multiplexers and the

corresponding test time is provided.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391.

The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

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